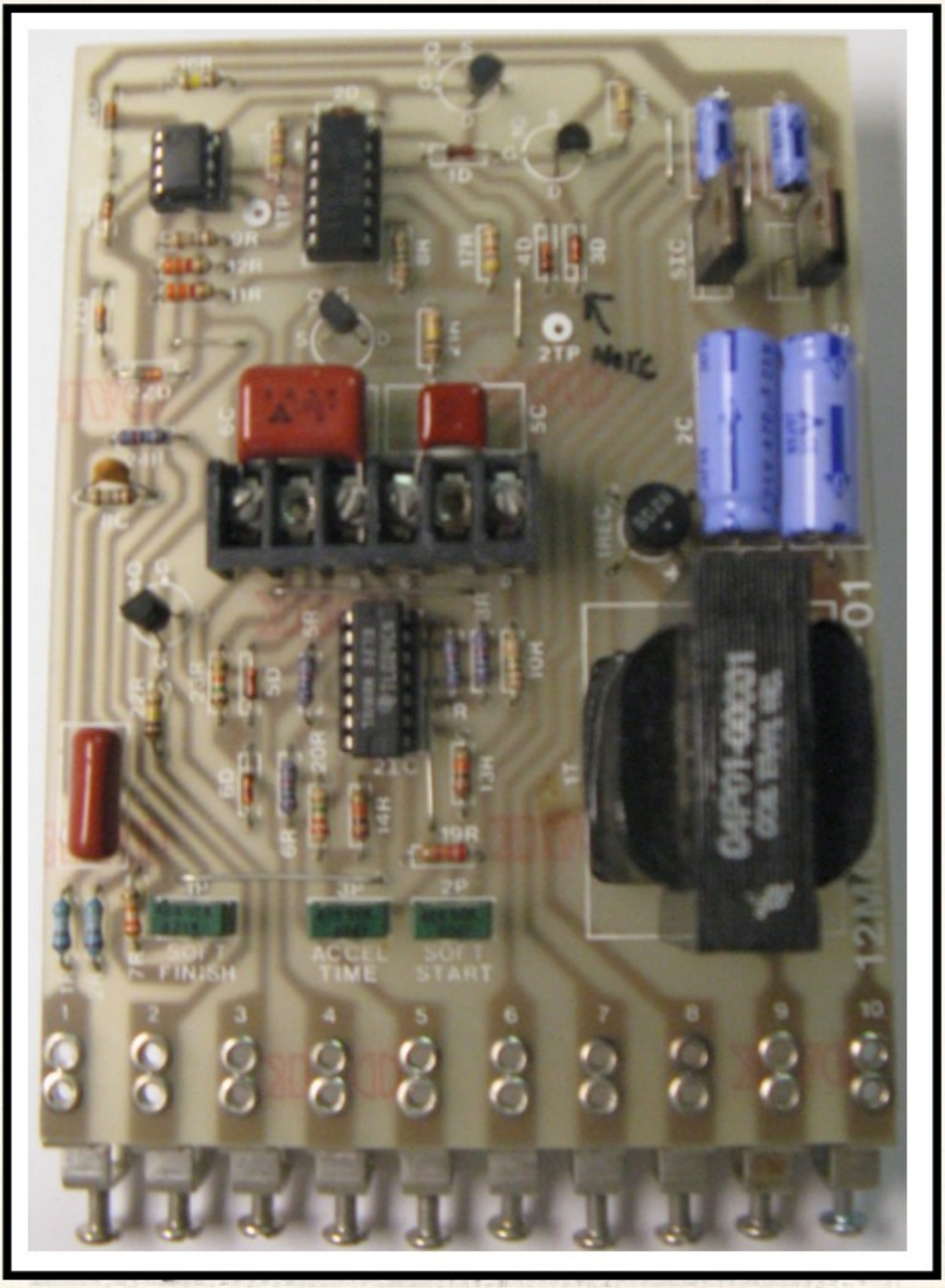
Trouble-shooting Manual
MODEL 238 S-CURVE RAMP GENERATOR
PART NUMBER 12M03-00127-01



GEMINI MODEL 238 S-CURVE RAMP GENERATOR

PART NUMBER 12M03-00127-01
SCHEMATIC DIAGRAM 12M03-00127-01

I. SPECIFICATIONS

SUPPLY
- 120 volts AC ± 10%
- 50/60 Hz, single phase

AMBIENT TEMPERATURE
- 0° to 40°C (32° to 104°F)
- 50°C in cabinet

INPUT
- 0 to Positive or Negative 6V DC @ 0.6 mA (10 K ohms)

OUTPUT
- NON-INVERTED: 0 to Positive or Negative 6V DC @ 5mA
- INVERTED: 0 to Negative or Positive 6V DC @ 5mA. Both inverted and non-inverted outputs are bipolar

TIMING ADJUSTMENT RANGE
- 12 seconds standard, adjustable over 6 to 1 ratio. Time is dependent on value of 6C (12 seconds per microfared) and can be modified accordingly.

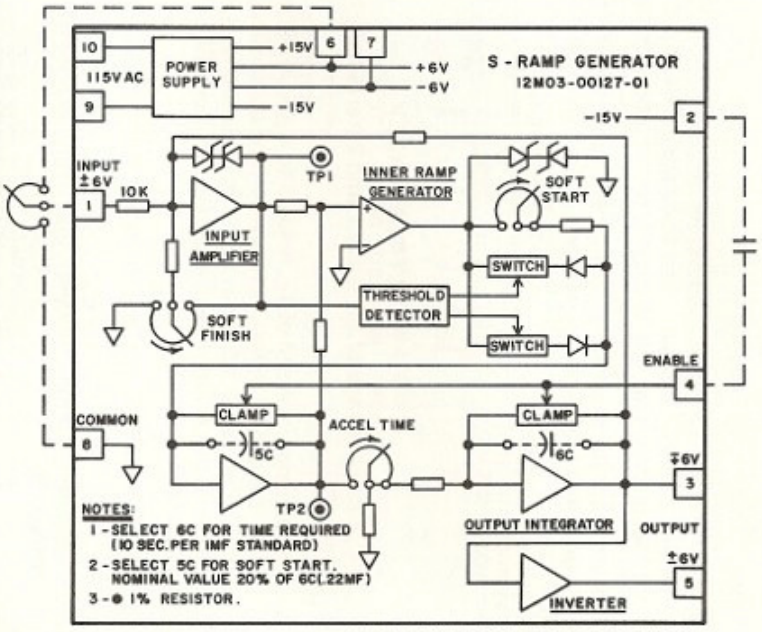


FIGURE 1 SIMPLIFIED SCHEMATIC

II. THEORY OF OPERATION

The REFLEX Model 238 S-Curve Ramp Generator converts step changes in input to a linear timed ramp at the output, but with the added capability of providing gradual onset (Soft Start) and ending (Soft Finish), each independently adjustable. With suitable adjustment the output voltage as a function of time assumes an "S" shape. This type of acceleration pattern is useful in applications where the load may be sensitive to rapid changes of acceleration. Typical pattern variations are shown in Figure 2.

It consists of the following elements as shown in the Simplified Schematic Diagram (Figure 1):

1. Power Supply
2. Input Amplifier
3. Inner Ramp Generator
4. Threshold Detector
5. Solid-State Switches
6. Output Integrator
7. Inverter

1. **Power Supply** – The power supply uses a center-tapped transformer with 10 volts on each side of center together with a bridge rectifier and two 470 MF filter capacitors to provide a nominal positive and negative unregulated 15 volts DC with respect to the transformer center-tap, which is connected to circuit common.

   Additionally, a positive and negative 6 volt regulated voltage is obtained from the positive and negative 15 volt supplies, using regulators 4IC and 5IC each with a 10 MF filter capacitor.

2. **Input Amplifier** – (IA) To operate the circuit an "Enable" signal of 15 volts negative from any source must be applied to terminal 4.

   The IA together with the Output Integrator (OI) acts as a conventional linear ramp generator, where the input and output voltages are compared at the summing junction of the IA (pin 2 of 1IC). When these two voltages are not equal, the IA swings to its maximum output, providing a signal of constant magnitude to the OI resulting in a linear rate of change of output voltage.

   However, the output of the IA is not fed directly to the OI as it would be in a conventional integrating circuit. Instead, the output voltage is modified by the Inner Ramp Generator. Additionally, adjustable feedback from the output of the IA to its own input modifies its gain from essentially infinite to as low as approximately 3 to 1.

3. **Inner Ramp Generator (IRG)** – The IRG consists of op-amp 2IC(A) and (B) and associated components and is responsible for the soft start to an output ramp voltage that would otherwise be linear. For the description of its operation assume that the "Soft Finish" potentiometer is turned to zero (CCW).

   With the conventional linear ramp generator the signal supplied to the Output Integrator is a constant value determined by the voltage limit of the Input Amplifier. With a constant input voltage the Output Integrator produces a linear ramp output.

   The IRG acts between the output of the Input Amplifier and the input to the Output Integrator to produce an integrating signal which starts at zero and increases linearly to the same value as the output of the Input Amplifier.

   The result is that the Output Integrator starts with a zero slope corresponding to the initial output from the IRG and gradually increases in slope as the output of the IRG increases. When the output of the IRG has reached a value equal to the limited output of the Input Amplifier it remains at this value and the Output Integrator continues its ramp at the same linear rate as would be obtained if the Input Amplifier were connected directly to the Output Integrator.

   When the output ramp has reached a voltage equal to the input voltage, it stops increasing. This is accomplished because the output voltage of the Input Amplifier drops to zero when the feedback from the output of the Output Integrator through 24R becomes equal to the reference input through 1R and 2R.

   The output of the IRG also returns to zero in response to its input from the Input Amplifier. Under these circumstances, however, it is undesirable for the rate at which it returns to zero to be extended by a ramp generator. The IRG is therefore allowed to operate almost instantaneously by the action of one of the Solid State Switches as described in detail later.

   When either switch is "closed" the timing function of the IRG is disabled for one direction of change determined by polarity of diodes 3D and 4D. The output of the IRG therefore can immediately follow input changes in this direction.

   The "Soft Finish" is a gradual reduction in the rate of change of the output ramp voltage as it approaches its final value. To accomplish this, it is necessary to gradually decrease the input signal to the Output Integrator.

   Feedback around the Input Amplifier, 1IC, is adjusted by the "Soft Start" potentiometer so that the output of the Input Amplifier becomes a function of the difference between its input and output voltages.

   As the magnitude of the output voltage approaches that of the input and the difference becomes smaller, the output of the Input Amplifier also becomes smaller. Since the IRG is controlled by one of the Solid State Switches to allow the immediate response to a reduction in Input Amplifier output, it passes the reduced voltage directly to the Output Integrator and the rate diminishes. This rate continues to become smaller as the difference between the input and output approaches zero. When there is no difference the circuit stabilizes with input and output being equal.

   The Output Integrator provides an output polarity at Terminal 3, opposite to that of the input polarity (Inverted) at Terminal 1.

4. **Threshold Detector** – The Threshold Detector consists of two comparators, 3IC(A) and (B), connected to detect when the output of the Input Amplifier is more than 50mV nominal in either direction.

   In the absence of any output from 1IC, both comparator outputs are negative. This "opens" both Solid State Switches. If the output of 1IC becomes positive 3IC(B) will "close" Switch 1Q and if the output of 1IC becomes negative 3IC(A) will "close" Switch 2Q.

   Each Threshold Detector thus closes the proper Solid State Switch for a given polarity of output from 1IC to allow instantaneous decrease in signal to the Output Integrator. At the same time, the other Solid State Switch remains open allowing the ramp action of the IRG for *increases* in the output of the Input Amplifier.

5. **Solid State Switches** – The FET switches, 1Q and 2Q, coordinate the action of the Threshold Detector and Inner Ramp Generator as described above.

6. **Output Integrator** – The Output Integrator, 2IC(C), charges capacitor 6C at a rate determined by the magnitude of the signal from the Inner Ramp Generator. This magnitude is adjusted by "ACCEL TIME" adjustment, 3P, to provide a nominal 6 to 1 range (2 to 12 seconds per microfarad of capacitor 6C) for the linear portion of the ramp output.

   Ramp times associated with the "Soft Start" and "Soft Finish" must be added to the basic linear time. The "Soft Start" is determined by the value of 5C and the adjustment of 2P. While the optimum value is best determined by trial and error, a good starting point is a value of 5C equal to 20 to 50% of the value of 6C.

   The effects of the "Soft Finish" adjustment, 1P, are a percentage of the full output, and therefore are automatically determined by the selection of 6C. Optimum settings again are best determined by trial and error.

   The output of the circuit is reduced to zero immediately on removal of the "Enable" signal (negative 15 volts on Terminal 4).

7. **Inverter** – The Inverter, 2IC(D), provides an output at Terminal 5 which has the same polarity (non-inverted) as the input at Terminal 1.

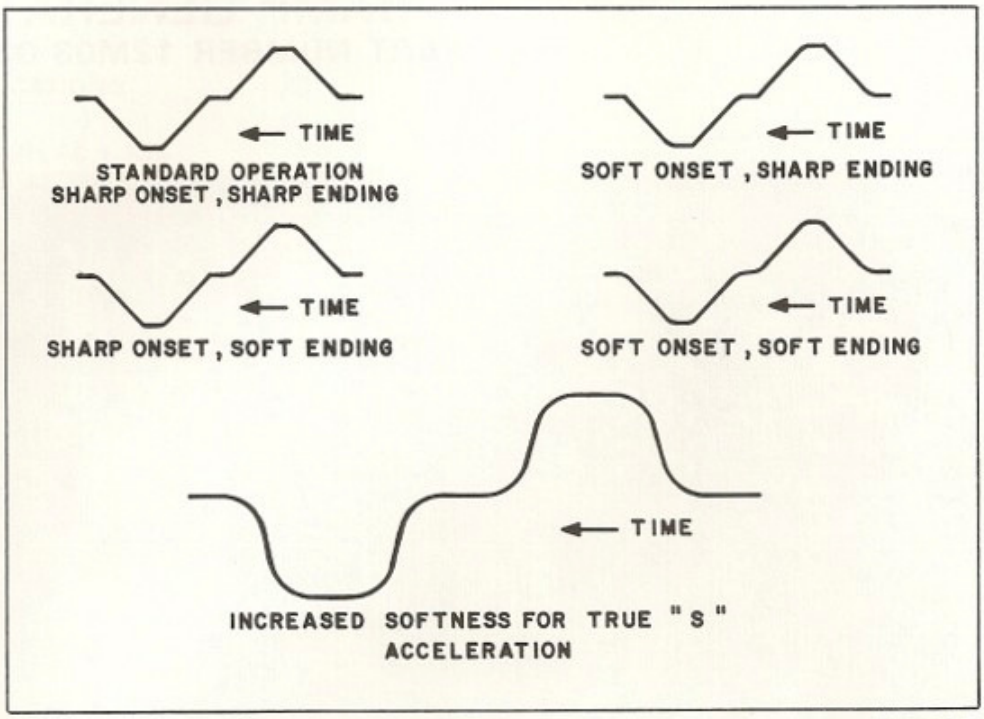


FIGURE 2

COMPONENT LIST - ASSEMBLY #12MO3-00127-01

Symbol	Part #	Description (Acceptable Substitute)*
1T	04P01-00001	Transformer-120VAC PRI, two 10V SEC @ 220mA (Signal PC20-220)
1 REC	05P01-00003	Rectifier Bridge-50V, 1A (EDI-PF50)
1-6D	05P02-00001	Diode-Signal, 50 mA, 200PIV (1N4148)
1-4ZD	05P03-00005	Zener Diode-6.8V, 500mW, 10%
1-4Q	05P05-00001	Transistor-N Channel JFET (2N4093)
1IC	05P08-00005	Precision Op-Amp-(Fairchild 714)
2IC	05P08-00002	Quad Op-amp (TI-TL084CN)
3IC	05P08-00004	Quad Comparator (National-LM339)
1P	02P04-10301-00	Potentiometer, 10K, ½W (Beckman-72XR10K)
2,3P	02P04-50301-00	Potentiometer, 50K, ½W (Beckman-72XR50K)
1,2C	03P01-47102-01	Capacitor-470MF, 25V, electrolytic
3,4C	03P01-10001-00	Capacitor-10MF, 16V, electrolytic
5C	03P07-22410-00	Capacitor-.22MF, 100V, film (Standard Value)
6C	03P07-10510-00	Capacitor-1.0MF, 100V, film (Standard Value)
7C	03P07-10510-00	Capacitor-1.0MF, 100V, film
8C	03P06-10305-00	Capacitor-.01MF, 50V ceramic
1,2R	01P02-49911-01	Resistor, 4.99K, ½W, 1%
3-6R,24R	01P02-10021-01	Resistor, 10.0K, ½W, 1%
7R	01P01-33300-02	Resistor, 33K, ¼W, 5%
8-10R	01P01-10500-02	Resistor, 1M, ¼W, 5%
11,12R	01P01-33200-02	Resistor, 3.3K, ¼W, 5%
13,14R	01P01-10300-02	Resistor, 10K, ¼W, 5%
15,16, 21,22R	01P01-10400-02	Resistor, 100K, ¼W, 5%
17,18R	01P01-47200-02	Resistor, 4.7K, ¼W, 5%
19R	01P01-22200-02	Resistor, 2.2K, ¼W, 5%
20R	01P01-22500-02	Resistor, 2.2M, ¼W, 5%
23R	01P01-15300-02	Resistor, 15K, ¼W, 5%
25R	01P01-10500-02	Resistor, 1M, ¼W, 5%
4IC	05P08-00006	+6 Volt regulator (7806)
5IC	05P08-00007	-6 Volt regulator (7906)

*OR EQUAL

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BENCH TEST

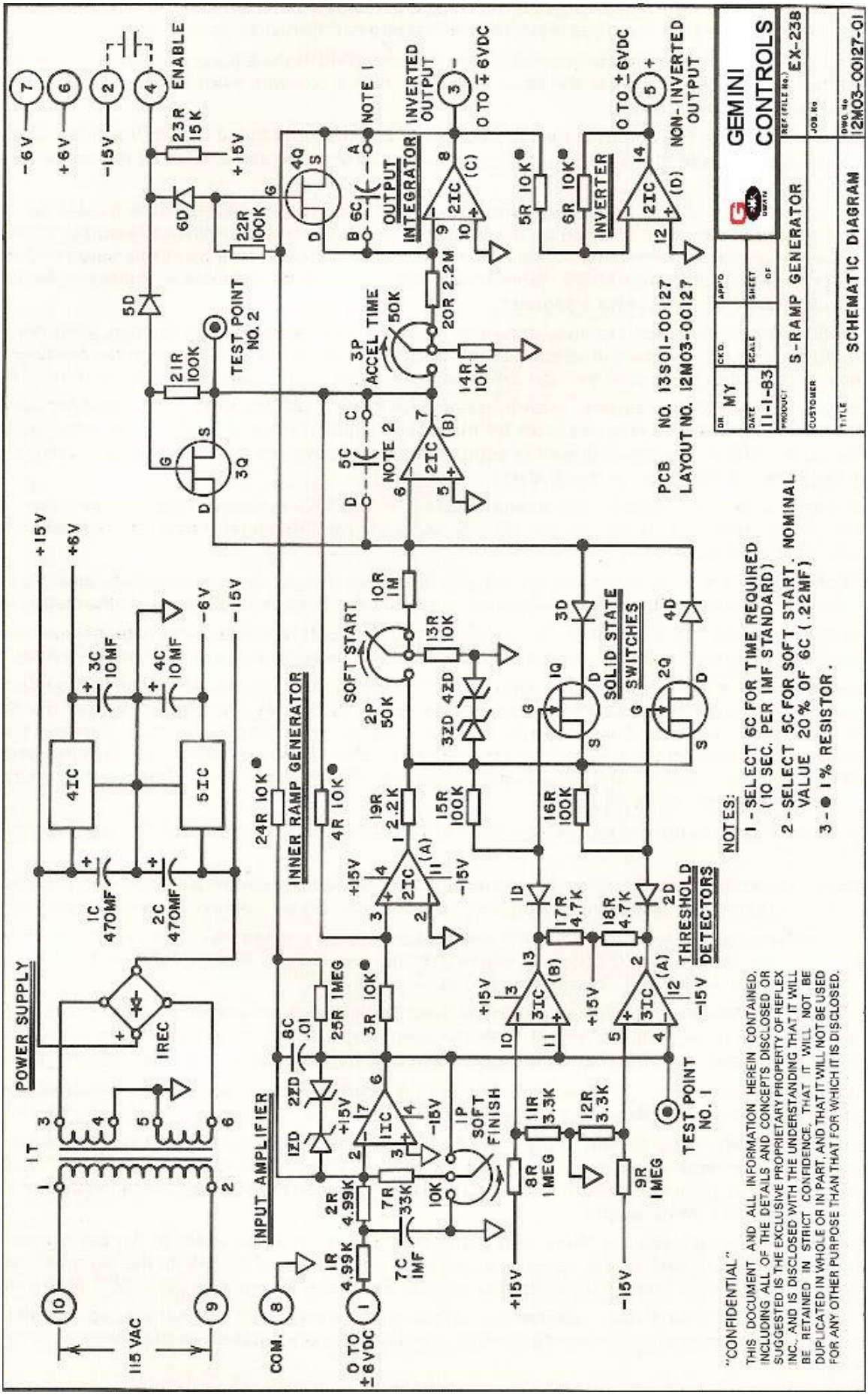
TEST MATERIAL REQUIRED:

1 – 120V AC line cord
2 – Test leads
1 – Oscilloscope (Tektronix 2213 or equal)

1. The following test is made using the factory supplied capacitors mounted on the internal capacitor terminal board. 5C is a 0.22 MFD film and 6C is a 1.0 MFD film.
2. Apply 120V AC power to terminals 9 and 10.
3. Apply a test lead between terminals 2 and 4 to "ENABLE" the circuit.
4. Connect an oscilloscope capable of slow horizontal sweep rates (1.0 or 0.5 seconds per division) to terminal 8 LO and terminal 5 HI. The horizontal should be set to sweep 1 division per second and the vertical should be set to read plus or minus 10V DC with the center being 0V DC. The trace should remain at 0V DC when connected to the unit under test.
5. Set all potentiometers to full CCW.
6. Using a second test lead, connect one end to terminal 1 and as the scope trace contacts one of the major dividers on the left side of the graticle, touch and hold the other end of the lead to terminal 6. The trace should immediately begin to rise linearly to about 6.8V DC and abruptly stop rising (without overshoot) at a point approximately 2.5 divisions (or seconds) from the starting point. Removing the test lead should have the same result, only going from 6.8V DC to 0V DC.
7. Repeat step 6 using terminal 7 instead of terminal 6. In this case the trace should descend to –6.8V DC and then return to 0V DC in the same time span (2.5 divisions or seconds).
8. Turn the "SOFT START" and "SOFT FINISH" potentiometers to full CW and repeat steps 6 and 7. This time the trace should gently begin and end its travel as if forming an "S" during upward travel and a reverse "S" while descending. The start and finish "S" portions should not be noticeably different. The total rise and fall times in this mode should be about 4.0 divisions or seconds.
9. Move the oscilloscope HI to terminal 3 and turn the "ACCEL TIME" potentiometer fully CW.
10. As the trace intersects the center of the graticle, touch and hold the jumper from pin 1 to pin 7. The trace should rise until it is near the center of the graticle two full sweeps later, or about 20 seconds.
11. With the trace at about +6.8V DC remove the jumper from either terminal 2 or terminal 4. The scope trace should immediately fall to 0V DC.

VOLTAGE CHECK

1. The primary voltage of 1T, leads 1 and 2 (terminals 10 and 9), should be 120V AC.
2. The secondary voltage of 1T, leads 3 to 4 and leads 5 to 6 should be 10V AC. These can be measured between circuit common, terminal 8 (leads 4 and 5), and each AC input to the bridge rectifier 1 REC (leads 3 and 6). Voltage at the AC input to the bridge rectifier 1 REC (leads 3 to 6) should be 20V AC.
3. +15V DC nominal between the positive end of capacitor 1C and terminal 8.
4. –15V DC nominal between the negative end of capacitor 2C and terminal 8.
5. +6V DC nominal (5.5 to 6.5 volts) between terminal 6 and terminal 8.
6. –6V DC nominal (5.5 to 6.5 volts) between terminal 7 and terminal 8.


GEMINI CONTROLS
S-RAMP GENERATOR
EX-238
SCHEMATIC DIAGRAM
12M03-00127-01
POWER SUPPLY
INPUT AMPLIFIER
INNER RAMP GENERATOR
OUTPUT INTEGRATOR
INVERTER
SOLID STATE SWITCHES
THRESHOLD DETECTORS
SOFT START
ACCEL TIME 50K
TEST POINT NO. 1
TEST POINT NO. 2
ENABLE
INVERTED OUTPUT
NON-INVERTED OUTPUT
115 VAC
COM.
0 TO ±6VDC
0 TO ∓6VDC
PCB NO. 13501-00127
LAYOUT NO. 12M03-00127
NOTES:
1 - SELECT 6C FOR TIME REQUIRED (10 SEC. PER 1MF STANDARD)
2 - SELECT 5C FOR SOFT START. NOMINAL VALUE 20% OF 6C (.22MF)
3 - ● 1% RESISTOR.
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